Listing of the Claims

1 and 2. (Canceled)

3. (Currently Amended) The memory ~~system~~ device of claim 32 [[1]], and further comprising a memory controller connected to the memory arrays ~~first array and to the second array~~, wherein ~~the~~ a first memory array operates at a first supply voltage and a ~~the~~ second memory array operates at a second supply voltage, wherein the second supply voltage is less than the first supply voltage so that the first memory array performs read and write operations faster than said memory second array, and wherein a length of the signal path from the second memory array to ~~a~~ said memory controller is less than a length of the signal path from the first memory array to the memory controller, such that, after a request for data, an output of a ~~the~~ first data packet ~~of a data word~~ from the first memory array and an output of a ~~the~~ second packet ~~of said data word~~ from the second memory array arrive at the memory controller at about the same time.

4. (Canceled)

5. (Currently Amended) The memory ~~system~~ device of claim 32 [[1]], and further comprising a memory controller connected to the memory arrays ~~first array and to the second array~~, wherein the first memory array comprises a wordline length that is shorter than a wordline length of the second memory array, and wherein a length of the signal path from the second memory array to a said memory controller is less than a length of the signal path from the first memory array to the memory controller, such that, after a request for data, an output of ~~the~~ a first data packet ~~of a data word~~ from the first memory array and an output of a ~~the~~ second data packet ~~of said data word~~ from the second memory array arrive at the memory controller at about the same time.

6. (Currently Amended) The memory ~~system~~ device of claim 5, wherein the first memory array is connected to an operating voltage that is different than an operating voltage connected to the second memory array.

7. (Currently Amended) The memory ~~system~~ device of claim 1, wherein the first memory array comprises sensing circuitry connected to and driven by a system supply voltage, and the second memory array comprises sensing circuitry connected to and driven by a ground potential such that the first memory array has a faster cycle time than the second memory array but the first array has a longer latency interval than the second memory array.

8-20. (Canceled)

21. (Currently Amended) The memory ~~system~~ device of claim 32 [[7]], and further comprising a memory controller connected to the memory arrays ~~first array and to the second array~~, wherein each memory array stores a byte ~~the first data packet stored in the first array is a byte and the second data packet stored in the second array corresponds to is a byte~~, and wherein the memory controller reads a multi-byte information packet from the ~~first and second~~ memory arrays by reading bytes stored each of the respective memory arrays ~~a first byte from the second array followed by reading a second byte from the first array followed by reading a third byte from the second array~~.

22. (Currently Amended) The memory ~~system~~ device of claim 32 [[1]], wherein ~~the first array~~ one of the memory arrays has a refresh rate and refresh current that is greater than a refresh rate and refresh current for another of the memory arrays ~~the second array~~.

23. (Currently Amended) The memory ~~system~~ device of claim 32 [[1]], wherein ~~the first array~~ a first memory comprises more cells per bitline than the number of cells per bitline of a second memory array ~~the second array~~.

24. (Currently Amended) The memory ~~system~~ device of claim 23, wherein the second memory array comprises at least two sub-arrays each having the same number of cells per bitline.

25-31. (Canceled)

32. (New) A memory device comprising:

multiple memory arrays operating at differing operating voltages and/or utilizing differing sense amplifier architectures compensated for by their physical placement for the purpose of optimizing power efficiency and such that data comprising a single read and/or write transaction at a point in time consists of data respectively read from and/or respectively written to said multiple memory arrays.